REMARKS

Present Status of the Application

Claims 1-4 remain pending, of which claim 1 has been amended to more clearly define the invention. It is believed no new matter is added by way of amendment to claim 1 or otherwise to the application. For at least the following reasons, Applicants respectfully submit that claims 1-4 are in proper condition for allowance. Reconsideration is respectfully requested.

Response to Rejections under 35 U. S. C. 102

1. The Office Action rejected claims 1 and 3-4 under 35 U. S. C. 102(b) as being anticipated by Yu et al. (US-5,869,873, hereinafter Yu).

Applicants respectfully disagree and traverse the above rejections as set forth below.

In response to argument filed June 5, 2002, the Office Action in paragraph 5, lines 5-6, states that the EPROM transistor is not cited as being the anti-latch up circuit, the RC circuit is cited as being the anti-latch up circuit. Applicants would like to point out that if EPROM is not cited as being the anti-latch up circuit, the RC circuit in Yu's Fig. 6 can not be the anti-latch up circuit either, because the EPROM provides no signal output to the SCR circuit so it cannot prevent the latch up of the SCR circuit. In the claimed invention, the RC circuit is one embodiment of the anti-latch up circuit and it provides a voltage (a high voltage in this case) to the third terminal of the SCR circuit to prevent it from latch up during normal operation because the third terminal can serve as the guard ring.

As recited in the amended claim 1, the sixth terminal of the anti-latch up circuit is coupled to the third terminal of SCR circuit, *whereby an anti-latch-up signal is sent from the sixth connection terminal to the SCR circuit.* The Office Action asserts that "the connection between the RC elements and the third connection terminal of the SCR circuit is done via transistor 4" (EPROM 4 in Yu's Fig. 6). Applicants respectfully disagree, and would like to point out that in Yu's invention, EPROM 4 is used to trigger SCR circuit due to its low breakdown voltage (col.4, line 60 – col.5, line10). It cannot provide any voltage to the third terminal of SCR circuit since it is in a normal off state (its control gate is ground via resistor R). Thus, the connection between the RC elements and the third connection terminal of the SCR circuit in Yu is different from the connection between the anti-latch-up circuit and the third terminal of SCR circuit of the present invention.

The Office Action on page 3, lines 3-5, states that although Yu does not state a voltage source, this feature is inherent in Yu's device as the line connecting the pad and the internal circuit is the voltage source. Note that the device would not function without a voltage source. Applicants respectfully disagree and would like to point out that if the internal circuit in Yu's Fig.6 is the voltage source, then the pad connecting to the internal circuit must not be an I/O pad! Rather it must be a power pad. The I/O pad is used to get a signal from the system into the internal circuit and output a signal to the system with the output driver. If it is connected to the voltage source, it will fail since the power pad cannot get or output any signal. In the claimed invention, however, the first terminal of SCR is coupled to the I/O pad and the fourth terminal of the anti-latch up circuit is coupled to the voltage source. In this arrangement, because a plurality of I/O pads only

needs one voltage source, only one anti-latch up circuit is used for a plurality of I/O pads, instead of one anti-latch up circuit for one pad. Therefore the area occupied by the anti-latch up circuit can be minimized, and the integration of the device can be effectively increased.

Further, the Office Action states that Yu's device would not function without a voltage source. However, Applicants would like to point out that in fact Yu's device can function without a voltage source since it only bypasses the ESD current from the pad to Vss, not Vcc (voltage source). If the internal circuit in Yu's Fig.6 is not the voltage source, Yu's device has no terminal coupled to the voltage source! That is, the voltage source has no effect on Yu's device if the internal circuit is not voltage source.

Therefore, a voltage source as recited in claim 1 is not inherent in Yu.

For at least the reasons discussed above, claim 1 is not anticipated by Yu and is patentable over Yu.

For at least the same reasons, dependent claims 3 and 4 are not anticipated by Yu and are patentable over Yu. In addition, these dependent claims contain features that further distinguish over the cited reference.

Claim 3 requires that the sixth connection terminal of the anti-latch up circuit be coupled to a second N+ doped region of the SCR circuit. The Office Action stated that in Yu's invention, RC circuit is also coupled to the second N+ region via transistor 55 (EPROM) as shown in Yu's Fig. 5& 6. Applicants respectfully disagree and would like to point out that in fact, the transistor 55 (EPROM) of Yu is in normally off state during the normal operation. Therefore, it couples nothing from RC circuit to the second N+ doped region of SCR circuit.

With regard to claim 4, according to Yu's description (col.5, line 24-40), RC circuit in Yu's Fig.6 is used to program "EPROM" to raise its threshold voltage from 0.7V to 1.1~2V during ESD event. That's why the output node of RC circuit is coupled to the control gate of EPROM, instead of the node 33 in Yu's Fig.6. In the claimed invention, however, RC circuit (one embodiment of the anti-latch up circuit) is used to avoid the latch up of SCR circuit by providing a voltage signal to the third terminal of SCR circuit during normal operation. Thus, its output terminal (sixth connection terminal in Claim1) is coupled to Node A instead of the control gate of EPROM. In fact, EPROM is needed to lower the trigger of SCR in Yu's invention but not in the claimed invention.

For at least the foregoing reasons, reconsideration of the rejection is respectfully requested.

Response to Rejections under 35 U. S. C. 103

2. The Office Action rejected claim 2 under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Ker et al. (US-5,754,380, hereinafter Ker).

Applicants respectfully disagree and would like to particularly point out that even though Ker is relied upon for showing a first diode and a second diode, still Ker cannot cure the specific deficiencies of Yu as discussed above. Accordingly, Applicants respectfully submit that claim 1 as well as its dependent claim 2 patently define over Yu and Ker. Reconsideration and withdrawal of the rejection is respectfully requested.

CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 1-4 are in proper condition for allowance. If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is cordially invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,
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Date: 11/5/2002

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Version with markings to show changes made

In The Claims

1. (Amended) An electrostatic discharge (ESD) protection circuit, suitable for use on the I/O pad; the ESD protection circuit comprising:

a silicon controlled rectifier (SCR) circuit, which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively connected to the I/O pad and a ground voltage, so as to discharge the electrostatic charges; and

an anti-latch-up circuit, which comprises a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal, respectively coupled to a voltage source, the ground voltage, and the third connection terminal of the SCR circuit, whereby an anti-latch-up signal is sent from the sixth connection terminal[, so that]to the SCR circuit[is not unexpectedly, causing latch-up of the ESD protection circuit].

Claims 2-4 remained as ever.